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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,038	01/29/2004	Haruo Nishida	118497	2578

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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	PAPER NUMBER
2117	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/766,038	NISHIDA ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *4-7,11-14 and 18-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,8-10 and 15-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Claims 1-3, 8-10 and 15-17, Species A, Figs. 1-5, in the reply filed on March 20, 2007 is acknowledged.

Claims 4-7, 11-14 and 18-21 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Species, there being no allowable generic or linking claim.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) to JAPAN 2003-022274 filed 01/30/2003. The certified copy has been filed in parent Application No. 10/766,038, filed 01/29/2004.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 01/29/2004 has been considered by the examiner, as indicated by the attached form PTO-1149.

Specification

The disclosure is objected to because of the following informalities:

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "An integrated circuit, a test circuit and a test method for performing transmission and reception processing to and from a first and a second macro block at a first clock frequency".

Appropriate correction is required.

Claim Objections

Claims 8-10 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claims 8-10, each recite an integrated circuit comprising the limitations of the first macro block, and the second macro block, which fail to further limit the parent claim, since these limitations are the same ones repeated in the parent claim.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 8-10, each recite an integrated circuit comprising the limitations of the first macro block, and the second macro block, which render the claims indefinite, because the limitations lack sufficient description.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3 and 15-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Cote et al. (US Patent No. 6,671,839) filed: June 27, 2002.

Regarding Claims 1, 15, Cote discloses a test controller 14 that performs transmission and reception processing between two embedded cores 16 and 18 having core test controllers 20 and 22, respectively, Fig. 1. A circuit 150 having two test controllers 152 and 154, for testing associated core logic 156 and 158, at speed corresponding to a first clock frequency, Fig. 7, where circuit 150 could be a subset of the circuit of FIG. 1.

In general, each of the test controllers 152 and 154 includes scan chains formed by serially connecting scannable memory elements in the core blocks, where each scan chain operates at application or design speed, allowing for simultaneous testing of multiple frequencies and multiple clocks. The test patterns are shifted into the scan chains. The output responses are captured and compacted into a signature in a manner well known in the art. The signature can be compared to a reference signature on-chip and a pass or fail response passed to the TAP, Figs. 2 and 7.

As shown in Fig. 5, waveform 100 is the test controller clock signal for at-speed test, derived from the system clock. Waveform 46 is the external test clock, ExtClock, which is typically a slower clock than the test controller clock. In this example, it is shown to be approximately four times slower.

Fig. 8 illustrates the timing of the two test controllers tested at speed, in parallel and having different clock frequencies as shown by waveforms 200 and 206, associated with a respective core logic 156 and 158.

As shown in Fig. 3, an expected signature register 50, also referred to as a shadow register, having a serial input 52 and a serial output 54 configurable in Hold mode for holding their contents constant and in Shift mode for shifting data through the register. The shadow register receives and holds the expected signature of test patterns, which are being executed, and, when the test patterns have completed executing, then the shadow register receives the actual signature from the signature register during a swapping operation. The expected signature is loaded into the shadow register while the corresponding test patterns are being executed. The test patterns are

executed at one clock rate and data is shifted through the shadow register at a different, usually slower, clock rate and for holding an expected signature until required, using the shift/Hold signal 66, as shown in Figs.3 and 5, where the Shift/Hold signal 66 is slower that the waveform 100 for at-speed test.

Regarding Claims 2, 3, 16, 17, with respect to claimed limitation of a loop-back mode, Cote discloses a test controller 14 that communicates with the two embedded cores 16 and 18 through the their respective core test controllers 20 and 22, respectively, which further includes a test access port (TAP) 24 for use in communicating with the core test controllers. The communication between the core test controllers and their respective cores is at-speed, while the communication between the core-test controllers anticipated and external test controller 14 is at slower a slower clock than the test controller clock.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques H. Louis-Jacques can be reached on 571) 272-4150. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

4/19/07

Date: 19 April 2007
Office Action: Non-Final Rejection

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